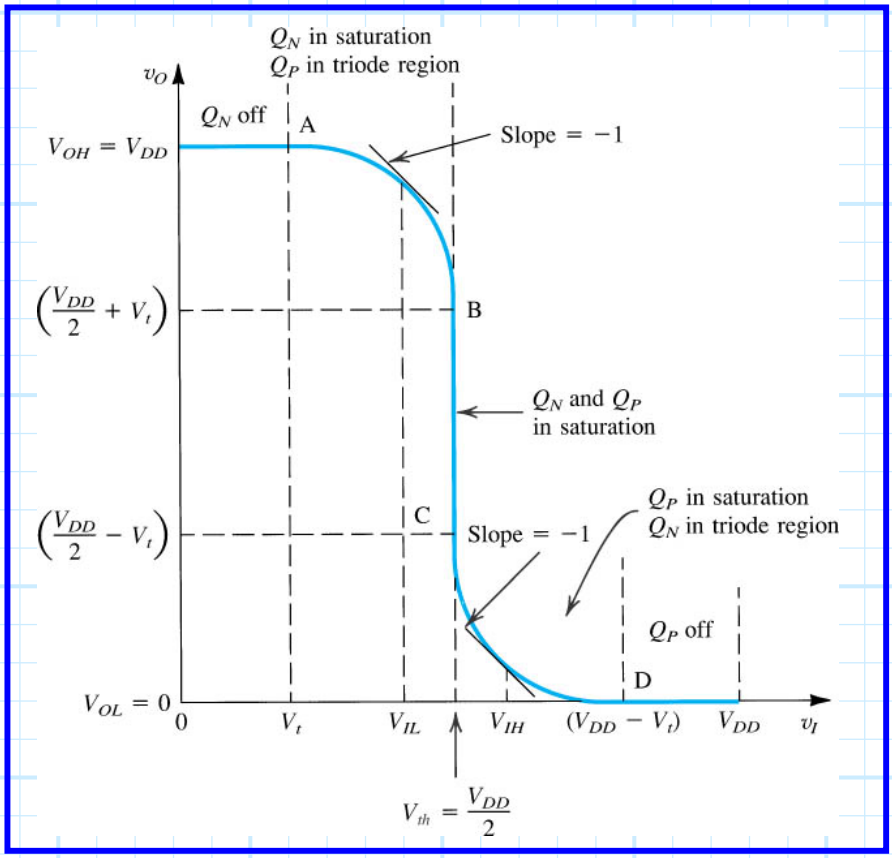
Peak CMOS Current

Q: *What do you mean, "**peak** CMOS current"? I thought that the drain current of a CMOS inverter was i_D=**0** ??*

A: The drain current i_D **is** zero specifically when v_I = 0 or v_I = V_{DD}. But, consider when v_I is some value **between** 0 and V_{DD}.



Note it is apparent from the **transfer function** that:

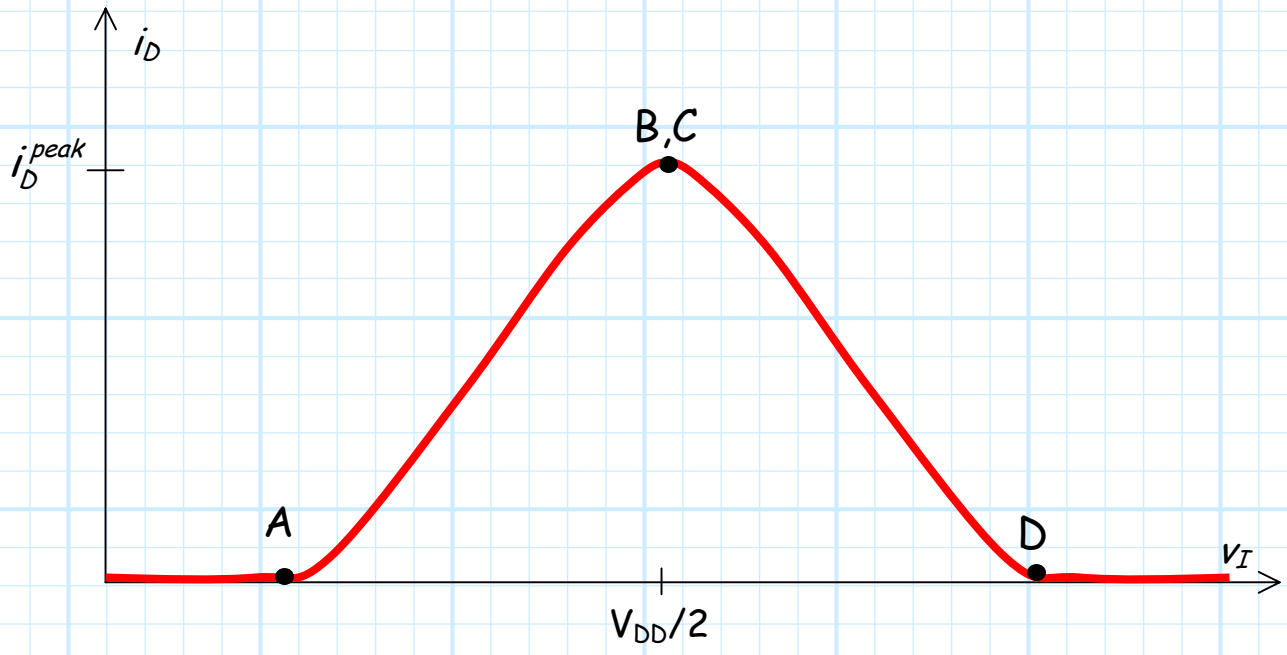
1. If $V_t < v_I < V_{DD}/2$, then Q_N is in *saturation* and Q_P is in **triode**.

2. If $v_I = V_{DD}/2$, then Q_N and Q_P are **both** in saturation.

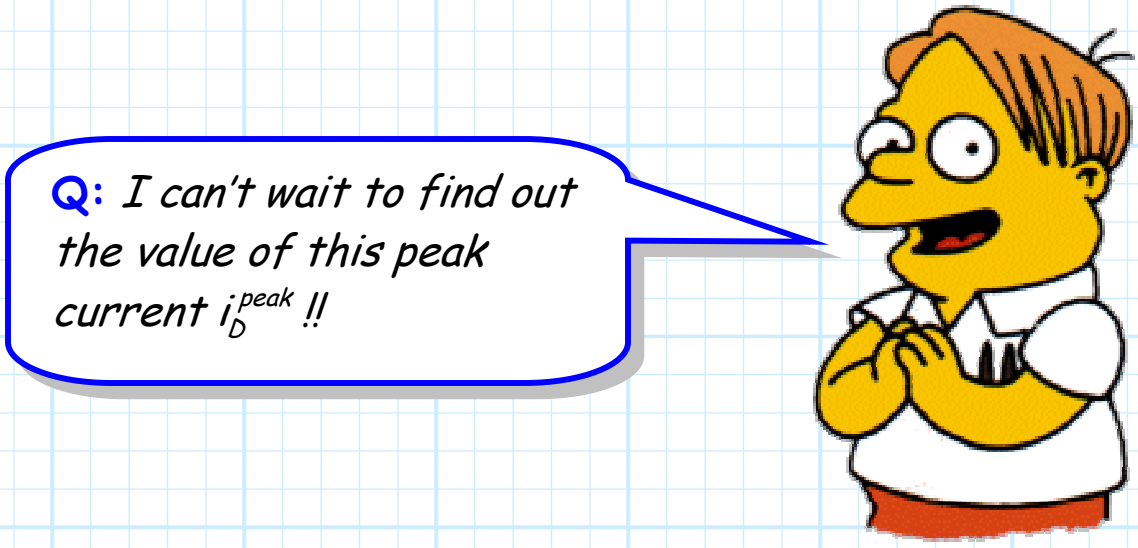
3. If $V_{DD}/2 < v_I < (V_{DD} - V_t)$, then Q_N is in **triode** and Q_P is in **saturation**.

Note that for each of these three cases, a **conducting channel** is present in **both** transistors Q_N and Q_P.

➡ The drain current i_D is therefore **non-zero** !!!



Note that the **peak current** i_D^{peak} occurs when $v_I = V_{DD}/2$.



A: The answer is rather **obvious**! The peak current occurs when $v_I = V_{DD}/2$. For that situation, we know that **both** transistor Q_N and Q_P are in **saturation**—and we **know** the current through a MOSFET when in saturation is:

" K times the excess gate voltage squared"

For **this** case, $v_{GSN} = v_I = V_{DD}/2$, thus:

$$\begin{aligned} i_D^{peak} &= K_n\left(v_{GSN} - V_{tn}\right)^2 \\ &= K\left(V_{DD}/2 - V_t\right)^2 \end{aligned}$$

If we wish to **minimize** the **dynamic** power dissipation P_D, then we need to **minimize** this current value (e.g., minimize K, or maximize V_t).